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(Use as many sheets as necessary)

Sheet	1	of	2
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Application Number	10/806,879
Filing Date	March 23, 2004
First Named Inventor	Hocevar
Art Unit	
Examiner Name	
Attorney Docket Number	TI-36180

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Examiner Signature	/R Stephen Dildine/
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Date Considered	08/02/2006
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Complete if Known	
		Application Number	10/806,879
		Filing Date	March 23, 2004
		First Named Inventor	Hocevar
		Art Unit	
		Examiner Name	
Attorney Docket Number	T1-36160		
Sheet	2	of	2

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ZHANG et al. "VLSI Implementation-Oriented (3,k)-Regular Low-Density Parity-Check Codes", IEEE Workshop on Signal Processing Systems (Sept.2001), pp.25-36.	

Examiner Signature	<i>R. Scott Feldner</i>	Date Considered	8/2/06
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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 3**Complete if Known**

Application Number	
Filing Date	
First Named Inventor	Hocevar
Art Unit	
Examiner Name	
Attorney Docket Number	TI-36160

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
RSD		US- 2004/0034828A1	02-19-2004	Hocevar	all
RSD		US- 5406570	04-11-1995	Berrou et al.	all
RSD		US- 5446747	08-29-1995	Berrou et al.	all
RSD		US- 5563897	10-08-1996	Pyndiah et al.	all
RSD		US- 5630156	05-13-1997	Privat et al.	all
RSD		US- 6023783	02-08-2000	Divsalar et al.	all
RSD		US- 6065147	05-16-2000	Pyndiah et al.	all
RSD		US- 6108388	08-22-2000	Douillard et al.	all
RSD		US- 6119264	09-12-2000	Berrou et al.	all
RSD		US- 6122763	09-19-2000	Pyndiah et al.	all
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				

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Signature

/R Stephen Dildine/

Date
Considered

08/02/2006

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		Application Number	
		Filing Date	
		First Named Inventor	Hocevar
		Art Unit	
		Examiner Name	
Sheet	2	of	3
		Attorney Docket Number	TI-36160

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
RSD		TANNER, et al., "A Class of Group-Structured LDPC Code", ISTA-2001 Proc. (Ambleside, England, 2001).	
RSD		RICHARDSON, et al., "Design of Capacity-Approaching Irregular Low-Density Parity Check Codes", IEEE Trans. on Information Theory, Vol. 47, No. 2 (Feb. 2001), pp. 619-637.	
RSD		RICHARDSON, et al., "Efficient Encoding of Low-Density Parity-Check Codes", IEEE Trans. on Information Theory, Vol. 47, No. 2 (Feb. 2001), pp. 638-56.	
RSD		ZHANG, et al., "VLSI Implementation-Oriented (3,k)-Regular Low-Density Parity-Check Codes", IEEE Workshop on Signal Processing Systems (Sept. 2001), pp. 25-36.	
RSD		BOUILLON, et al., "Decoder-First Code Design", Proc.: Int'l Symp. on Turbo Codes and Related Topics (Brest, France, Sept. 2001).	
RSD		SRIDHARA, et al., "Low Density Parity Check Codes from Permutation Matrices", 2001 Conference on Information Sciences and Systems (Johns Hopkins University, March 12, 2001)	
RSD		LI, et al., "Generalized Product Accumulate Codes: Analysis and Performance", Global Communications Conference (Globecom)(IEEE, 2001), pp. 975-79.	
RSD		MANSOUR, et al., "Turbo Decoder Architectures for Low-Density Parity Check Codes", Global Communications Conference (Globecom) (IEEE, 2002), pp. 1383-88.	
RSD		MANSOUR, et al., "On the Architecture-Aware Structure of LDPC Codes from Generalized Ramanujan Graphs and their Decoder Architectures", 2003 Conf. Inf. Sci. (Mar. 12, 2002).	
RSD		CHUNG et al., "Analysis of Sum-Product Decoding of Low-Density Parity-Check Codes using a Gaussian Approximation", Trans. Inf. Theory, V. 47, No. 2 (IEEE, Feb. 2001), 657-70.	

Examiner Signature	/R Stephen Dildine/	Date Considered	08/02/2006
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		Application Number	
		Filing Date	
		First Named Inventor	Hocevar
		Art Unit	
		Examiner Name	
Sheet 3	of 3	Attorney Docket Number	TI-36160

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RSD		GALLAGER, Low-Density Parity-Check codes (MIT Press, 1963).	
RSD		MACKAY, et al., "Comparison of Constructions of Irregular Gallager Codes", Trans. Comm., Vol. 47, No. 10 (IEEE, Oct. 1999), pp. 1449-54.	

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